REMARKS/ARGUMENTS

The Applicant HAS carefully considered this application in connection with the Examiner's Action and respectfully requests reconsideration of this application in view of the following remarks.

The Applicant originally submitted Claims 1-33 in the application. Presently, the Applicant has amended Claims 1, 7, 12, 17, 21, 22 and 27 and has canceled Claim 33. Additionally, no claims have been added. Accordingly, Claims 1-32 are currently pending in the application.

I. Formal Matters and Objections

The Examiner has objected to the Title as not being descriptive of the claimed invention. Accordingly, the Applicant has amended the Title to more clearly describe that claimed by the present invention. The Applicant appreciates the Examiner's diligence in finding and bringing this error to his attention.

The Examiner has also objected to the drawings as failing to include all the features of the invention specified in the claims. Namely, the Examiner has objected to the drawings as failing to show that claimed in Claims 33, as well as Claims 2 and 28. Accordingly, the Applicant has canceled Claim 33. It should be noted, however, that the Applicant disagrees with the Examiner that such features were not shown.

Regarding Claims 2 and 28, the Applicant is of the opinion that the isolation region is shown adjacent the semiconductor substrate. While the Examiner is of the opinion that the isolation region is within the semiconductor substrate, the Applicant asserts that the isolation region is formed within a trench located in the semiconductor substrate. Accordingly, it is not within the semiconductor substrate, but within a trench formed in the semiconductor substrate. Accordingly,

the isolation region is adjacent the semiconductor substrate. If the Examiner still disagrees with the Applicant, the Applicant requests that the Examiner call the Attorney of Record to discuss a change that is agreeable to both parties.

II. Rejection of Claims 2 and 28 under 35 U.S.C. §112, first paragraph

The Examiner has rejected Claims 2 and 28 under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. As recited in the objection above, the Applicant disagrees that Claims 2 and 28 include claim language that is unclear. According to the response to the objection above, the Applicant requests the Examiner withdraw this rejection.

III. Rejection of Claim 22 under 35 U.S.C. §112, second paragraph

The Examiner has rejected Claim 22 under 35 U.S.C. §112, second paragraph, as having antecedent basis problems. Accordingly, the Applicant has amended Claim 22 to correct this error. The Applicant requests the Examiner withdraw this rejection.

IV. Rejection of Claims 1-4, 7-9, 12, 13, 16, 17, 18, and 21-24 under 35 U.S.C. §102

The Examiner has rejected Claims 1-4, 7-9, 12, 13, 16, 17, 18, and 21-24 under 35 U.S.C. §102(b) as being clearly anticipated by U.S. Patent No. 5,391,907 to Jang (Jang). Presently, newly amended independent Claims 1, 7, 12, 17, 21, and 27 include the element that at least a portion of a source/drain region is located on the isolation region, but not in the semiconductor substrate. Jang fails to disclose such an element. Jang does disclose that its entire source/drain region 20 is diffused

within its semiconductor substrate 1, however, as the Examiner is quite aware, such a teaching is very different from the claimed subject matter. Accordingly, Jang fails to disclose that at least a portion of a source/drain region is located on the isolation region, but not in the semiconductor substrate.

Therefore, Jang does not disclose each and every element of independent Claims 1, 7, 12, 17, 21 and 27, and as such, is not an anticipating reference. Because Claims 2-4, 8-9, 13, 16, 18, and 22-24 are dependent upon Claims 1, 7, 12, 17, 21 and 27, Jang also cannot be an anticipating reference for Claims 2-4, 8-9, 13, 16, 18, and 22-24. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to these Claims.

V. Rejection of Claims 1-4, 6, 7-9, 11, 21-24, 26, 27-30, and 32 under 35 U.S.C. §102

The Examiner has rejected Claims 1-4, 6, 7-9, 11, 21-24, 26, 27-30, and 32 under 35 U.S.C. §102(e) as being clearly anticipated by U.S. Patent No. 6,246,094 B1 to Wong, *et al.* (Wong). As previously recited, newly amended independent Claims 1, 7, 12, 17, 21, and 27 include the element that at least a portion of a source/drain region is located on the isolation region, but not in the semiconductor substrate. Wong fails to disclose such an element. Wong does disclose that its source/drain regions 18, 20 are entirely diffused within its semiconductor substrate 10, however, as the Examiner is quite aware, such a teaching is very different from the claimed subject matter. Accordingly, Wong fails to disclose that at least a portion of a source/drain region is located on the isolation region, but not in the semiconductor substrate.

Therefore, Wong does not disclose each and every element of independent Claims 1, 7, 12, 17, 21 and 27, and as such, is not an anticipating reference. Because Claims 2-4, 6, 8-9, 11, 22-24, 26, 28-30, and 32 are dependent upon Claims 1, 7, 12, 17, 21 and 27, Wong also cannot be an

anticipating reference for Claims 2-4, 6, 8-9, 11, 22-24, 26, 28-30, and 32. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to these Claims.

VI. Rejection of Claims 1-4, 7-9, 21-24, and 27-30 under 35 U.S.C. §102

The Examiner has rejected Claims 1-4, 7-9, 21-24, and 27-30 under 35 U.S.C. §102(b) as being clearly anticipated by U.S. Patent No. 5,877,046 to Yu, *et al.* (Yu). As previously recited, newly amended independent Claims 1, 7, 12, 17, 21, and 27 include the element that at least a portion of a source/drain region is located on the isolation region, but not in the semiconductor substrate. Yu fails to disclose such an element. Yu does disclose that its source/drain regions 84, 82 are entirely diffused within its semiconductor substrate 70, however, as the Examiner is quite aware, such a teaching is very different from the claimed subject matter. (Column 6, lines 15-55). Accordingly, Yu fails to disclose that at least a portion of a source/drain region is located on the isolation region, but not in the semiconductor substrate.

Yu further fails to disclose that its isolation region 72 is formed within a trench located within the semiconductor substrate. As understood in reading Column 5, lines 39-60 of the Yu reference, Yu teaches that its electrically insulating layer 72 is formed on a first face of the first semiconductor substrate 70, then patterned resulting in the electrically insulating layers 72. Accordingly, Yu fails to disclose that its isolation region 72 is formed within a trench located within the semiconductor substrate 70.

Therefore, Yu does not disclose each and every element of independent Claims 1, 7, 12, 17, 21 and 27, and as such, is not an anticipating reference. Because Claims 2-4, 8-9, 22-24, and 28-30 are dependent upon Claims 1, 7, 12, 17, 21 and 27, Yu also cannot be an anticipating

reference for Claims 2-4, 8-9, 22-24, and 28-30. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to these Claims.

VII. Rejection of Claims 1-4, 7-9, 12-13, 16, 17-18, 21-24, 27-30 and 33 under 35 U.S.C. §102

The Examiner has rejected Claims 1-4, 7-9, 12-13, 16, 17-18, 21-24, 27-30 and 33 under 35 U.S.C. §102(b) as being clearly anticipated by U.S. Patent No. 4,551,743 to Murakami (Murakami). As previously recited, newly amended independent Claims 1, 7, 12, 17, 21, and 27 include the element that at least a portion of a source/drain region is located on the isolation region, but not in the semiconductor substrate. Murakami fails to disclose such an element. Murakami does disclose that its source/drain regions 19, 20 are entirely diffused within its semiconductor substrate 10, however, as the Examiner is quite aware, such a teaching is very different from the claimed subject matter. Accordingly, Murakami fails to disclose that at least a portion of a source/drain region is located on the isolation region, but not in the semiconductor substrate.

Therefore, Murakami does not disclose each and every element of independent Claims 1, 7, 12, 17, 21 and 27, and as such, is not an anticipating reference. Because Claims 2-4, 8-9, 12-13, 16, 18, 22-24, 28-30 and 33 are dependent upon Claims 1, 7, 12, 17, 21 and 27, Murakami also cannot be an anticipating reference for Claims 2-4, 8-9, 12-13, 16, 18, 22-24, 28-30 and 33. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to these Claims.

VII. Rejection of Claims 1-32 under 35 U.S.C. §102

The Examiner has rejected Claims 1-32 under 35 U.S.C. §102(b) as being clearly anticipated by Japanese Patent No. 11-274483A to Tsuchiaki (Tsuchiaki). As previously recited, newly amended independent Claims 1, 7, 12, 17, 21, and 27 include the element that at least a portion of a source/drain region is located on the isolation region, but not in the semiconductor substrate. Tsuchiaki fails to disclose such an element.

First, it is the position of the Applicant that the so called elevated source drain parts 23a, 26a that the Examiner states are source drain regions are actually just contacts for the source drain regions 21, 22, 24, 25. In support of this position, the elevated source drain parts 23a, 26a are the only electrically conductive structure shown for contacting the source drain regions 21, 22, 24, 25. Accordingly, the elevated source drain parts 23a, 26a are just source drain region interconnects.

Second, if what the Examiner states is true about the elevated source drain parts 23a, 26a, which as stated above the Applicant strongly disagrees with, the elevated source drain parts 23a, 26a are not located on the isolation region 12. As illustrated in each Figure of the Tsuchiaki reference, an oxide 13 is always located between the shallow isolation trench 12 and the so called elevated source drain parts 23a, 26a. Accordingly, Tsuchiaki fails to disclose that at least a portion of a source/drain region is located on the isolation region, but not in the semiconductor substrate.

Therefore, Tsuchiaki does not disclose each and every element of independent Claims 1, 7, 12, 17, 21 and 27, and as such, is not an anticipating reference. Because Claims 2-6, 8-11, 13-16, 18-20, 22-26, and 28-32 are dependent upon Claims 1, 7, 12, 17, 21 and 27, Tsuchiaki also cannot be an anticipating reference for Claims 2-6, 8-11, 13-16, 18-20, 22-26, and 28-32. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to these Claims.

VIII. Rejection of Claims 27-30 and 33 under 35 U.S.C. §103

The Examiner has rejected Claims 27-30 and 33 under 35 U.S.C. §103(a) as being obvious over Jang in view of the Applicant's admitted prior art (APA). As recited above, Jang fails to disclose every element recited in independent Claims 1, 7, 12, 17, 21 and 27. Namely, Jang fails to disclose that at least a portion of the source/drain region is located on the isolation region, but not in the semiconductor substrate.

Similarly, it is the position of the Applicant that Jang also fails to suggest the element that at least a portion of the source/drain region is located on the isolation region, but not in the semiconductor substrate. Jang fails to suggest such an element because Jang is focused on forming its source/drain regions in its semiconductor substrate using a diffusion process. Given the structure illustrated and described in Jang, as well as the method taught to manufacture such a device, one skilled in the art would not be motivated to place at least a portion of the source/drain region on the isolation region, but not in the semiconductor substrate. The structure taught and suggested by Jang always places its source/drain regions entirely within the semiconductor substrate. Accordingly, Jang fails to teach or suggest such an element.

The Examiner is using the APA for the sole proposition that interconnects may be used to connect the claimed device to various other active and passive devices. Notwithstanding the merits of the Examiner's proposition, the APA also fails to teach or suggest the element that at least a portion of a source/drain region is located on the isolation region, but not in the semiconductor substrate. A teaching or suggestion of an interconnect connecting various devices is dissimilar to a teaching or suggestion that at least a portion of a source/drain region is located on the isolation region, but not in the semiconductor substrate.

Therefore, the combination of Jang and the APA fails to teach or suggest each and every element of independent Claims 1, 7, 12, 17, 21 and 27, and as such, it fails to establish a *prima facie* case of obviousness with respect to independent Claims 1, 7, 12, 17, 21 and 27, and any claims dependent therefrom.

In view of the foregoing amendments and remarks, the cited references do not support the Examiner's rejection of Claim 27-30 and 33 under 35 U.S.C. §103(a). The Applicant therefore respectfully requests the Examiner withdraw the rejection.

IX. Rejection of Claim 33 under 35 U.S.C. §103

The Examiner has rejected Claim 33 under 35 U.S.C. §103(a) as being obvious over Wong in view of the Applicant's admitted prior art (APA). As recited above, Claim 33 was canceled without prejudice or disclaimer. Accordingly, the Applicant requests the Examiner withdraw this rejection.

X. Rejection of Claim 33 under 35 U.S.C. §103

The Examiner has rejected Claim 33 under 35 U.S.C. §103(a) as being obvious over Tsuchiaki in view of the Applicant's admitted prior art (APA). As recited above, Claim 33 was canceled without prejudice or disclaimer. Accordingly, the Applicant requests the Examiner withdraw this rejection.

XI. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-32.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

(1) Kindly replace the Title at the top of pages 1 and 30 with the following rewritten Title:

--[A SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE THEREFOR] A SEMICONDUCTOR DEVICE HAVING AT LEAST ONE SOURCE/DRAIN REGION FORMED ON AN ISOLATION REGION AND A METHOD OF MANUFACTURE THEREFOR--

IN THE CLAIMS

(1) Kindly rewrite Claim 1 as follows:

1. (Amended) A semiconductor device, comprising:

a semiconductor substrate;

a gate formed above the semiconductor substrate;

an isolation region located within a trench formed in the semiconductor substrate;

at least a portion of one of a source/drain region formed [above] on the isolation region, but not in the semiconductor substrate.

(2) Kindly rewrite Claim 7 as follows:

7. (Amended) A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

a trench located adjacent a side of the channel region;

an isolation region located in the trench; and

[a] at least a portion of one of a source/drain region located [over] on the isolation region, but not in the semiconductor substrate.

(3) Kindly rewrite Claim 12 as follows:

12. (Amended) A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

an isolation region located adjacent the channel region, the isolation region being located within a trench formed in the semiconductor substrate and not extending under the channel region; and

source/drain regions having a first portion located in the semiconductor substrate and a second portion located on the isolation region, but not in the semiconductor substrate.

(4) Kindly rewrite Claim 17 as follows:

17. (Amended) A semiconductor device, comprising:

a first transistor located adjacent a second transistor, wherein both the first and second transistors are located over a semiconductor substrate;

an isolation region located between the first and second transistors and within a trench located within the semiconductor substrate; and

source/drain regions associated with each of the first and second transistors, each of the source/drain regions having a first portion located in the semiconductor substrate and a second portion located on the isolation region, but not in the semiconductor substrate.

(5) Kindly rewrite Claim 21 as follows:

21. (Amended) A method of manufacturing a semiconductor device, comprising:

providing a semiconductor substrate;

creating a gate above the semiconductor substrate;

forming an isolation region within a trench located in the semiconductor substrate;

forming at least a portion of one of a source/drain region above the isolation region, but not in the semiconductor substrate.

(6) Kindly rewrite Claim 22 as follows:

22. (Amended) The method as recited in Claim 21 wherein forming an isolation region includes forming an isolation region adjacent to the semiconductor [region] substrate.

(7) Kindly rewrite Claim 27 as follows:

27. (Amended) An integrated circuit, comprising:

semiconductor devices, including;

a semiconductor substrate;

a gate formed above the semiconductor substrate;

an isolation region located within a trench formed in the semiconductor substrate;

at least a portion of one of a source/drain region formed above the isolation region, but not in the semiconductor substrate; and

interconnect structures contacting the semiconductor devices.

(8) Kindly cancel Claim 33 without prejudice or disclaimer.